PTO-1449 (Modified)	ATTY. DOCKET NO. RA001C11	SERIAL NUMBER 09/669,295
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	APPLICANT(S) FARMWALD ET AL.	
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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
GA	5,034,964	Jul.23, 1991	Khan et al	—	—	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
GA	SHO 58-192154	Nov. 9, 1983	Japan	—	—	NO	
GA	SHO 63-34795	Feb. 15, 1988	Japan	—	—	NO	
GA	SHO 61-107453	May 26, 1986	Japan	—	—	NO	
GA	SHO 63-91766	April 22, 1988	Japan	—	—	YES	
GA	SHO 62-16289	Jan. 24, 1987	Japan	—	—	NO	
GA	SHO 61-160556	Oct. 4, 1986	Japan	—	—	NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER Glenn Auve	DATE CONSIDERED 5/29/2001

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#6

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA001C11	SERIAL NUMBER 09/669,295
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	FILING DATE September 25, 2000	GROUP ART UNIT 2181

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,633,735	05/05/87	Novak, et. al			
	5,684,753	11/04/97	Hashimoto, et al			
	4,322,635	03/30/82	Redwine			
	5,006,982	04/09/91	Ebersole et al.			
	4,636,986	01/13/87	Pinkham			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

(1)	Ikeda, Hiroaki et al., "**100 MHz Serial Access Architecture for 4Md Field Memory**," Symposium of VLSI Circuits, Digest of Technical Papers, pp. 11-12 (Jun. 1990)
(2)	Takasugi, A. et al., "**A DATA TRANSFER ARCHITECTURE FOR FAST MULTI-BIT SERIAL ACCESS MODE DRAM**", 11TH European Solid State Circuits Conference, Toulouse France pp. 161-165 (Sep. 1985)
(3)	Ray Pinkham et al., "**A 128Kx8 70-MHz Multiport Video RAM with Auto Register Reload and 8x4 WRITE Feature**," IEEE Journal of Solid State Circuits, vol. 23, no. 3, pp. 1133-1139 (Oct. 1988)
(4)	Graham, Andy et al., "**Pipelined static RAM endows cache memories with 1-ns speed**", Electronic Design pp. 157-170 (Dec. 1984)
(5)	Robert J. Lodi et al., "**Chip and System Characteristics of a 2048-Bit MNOS-BORAM LSI Circuit**," IEEE International Solid-State Circuits Conference, (Feb. 1976)
(6)	Pinkham, Raymond, "**A High Speed Dual Port Memory with Simultaneous Serial and Random Mode Access for Video Applications**," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 6, pp. 999-1007 (Dec. 1984)
(7)	Ishimoto, S. et al., "**A 256K Dual Port Memory**," ISSCC Digest of Technical Papers, p. 38-39 (Feb. 1985)

EXAMINER Glenn Auve	DATE CONSIDERED 5/29/2001

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

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	FILING DATE September 25, 2000	GROUP ART UNIT 2181

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,979,145	12/18/90	Remington et al.			
	5,276,846	01/04/94	Aichelmann Jr., et. al			
	4,482,999	11/13/84	Janson et al.			
	5,029,124	07/02/91	Leahy et al.			
	5,193,193	03/09/93	Iyer			
	4,926,385	05/15/90	Fujishima et al.			
	4,566,099	01/21/86	Magerl			
	4,803,621	02/07/89	Kelly			
	4,589,108	05/13/86	Billy			
	4,870,622	09/26/89	Aria et al.			
	4,878,166	10/31/89	Johnson et al.			
	4,849,965	07/18/89	Chomel et al.			
	4,851,990	07/25/89	Johnson et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
	Sho 62-71428	10/05/88	JP			YES	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

(8)	Tomoji Takada et al., "**A Video Codec LSI for High-Definition TV Systems with One-Transistor DRAM Line Memories**," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1656-1659 (Dec. 1989)
(9)	Amitai, Z., "**Burst Mode Memories Improve Cache Design**," WESCON/90 Conference Record, pp. 29-32 (Nov. 1990)
(10)	Robert J. Lodi et al., "**MNOS-BORAM Memory Characteristics**," IEEE Journal of Solid-State Circuits, vol. SC-11, No. 5, pp. 622-631 (Oct. 1976)

EXAMINER Glenn Auvil	DATE CONSIDERED 5/29/2001

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,528,661	07/09/85	Bahr et al.			
	4,048,673	09/13/77	Hendrie et al.			
	4,519,034	05/21/85	Smith et al.			
	4,748,617	05/31/88	Drewlo			
	4,839,801	06/13/89	Nicely et al.			
	4,949,301	08/14/90	Joshi et al.			
	3,950,735	04/13/76	Patel			
	4,047,246	09/06/77	Kerllenevich et al.			
	5,029,124	07/02/91	Leahy et al.			
	4,763,249	08/09/88	Bomba et al.			
	4,625,307	11/25/86	Tulpule et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
	Sho 62-71428	10/05/88	JP			YES	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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#6

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,754,433	06/28/88	Chin et al.			
	5,023,488	06/11/91	Gunning			
	4,920,486	04/24/90	Nielson			
	4,719,602	01/12/88	Haq et al.			
	4,263,650	04/21/81	Bennet et al.			
	3,771,145	11/06/73	Wiener			
	3,691,534	09/12/72	Varadi et al			
	3,969,706	07/13/76	Proebsting et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

(1)	M. Horowitz et al., "MIPS-X: A 20-MIPS Peak 32-bit Microprocessor with on-Chip Cache", IEEE Journal of Solid State Circuits, vol. 22 No. 5, pp. 790-799 (Oct. 1987)
(2)	S Watanabe et. al., "An Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial READ/WRITE Mode", IEEE Journal of Solid State Circuits, vol. 24 No. 3, pp. 763-770 (June 1982)

EXAMINER Glenn Auve	DATE CONSIDERED 5/29/2001

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,766,536	08/23/88	Wilson, Jr. et al.	—	—	
	4,998,262	03/05/91	Wiggers	—	—	
	4,747,079	05/24/88	Yamaguchi	—	—	
	4,649,511	03/10/87	Gdula	—	—	
	4,757,473	07/12/88	Kurihara et al.	—	—	
	4,792,926	12/20/88	Roberts	—	—	
	4,811,202	03/07/89	Schabowski	—	—	
	4,860,198	07/22/89	Takenaka	—	—	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,445,204	04/24/84	Nishiguchi			
	4,821,226	04/11/89	Christopher et al.			
	4,882,712	11/21/89	Ohno et. al.			
	4,951,251	08/21/90	Yamaguchi et al.			
	4,928,265	~~12/29/97~~ 5/29/01 D	Beighe et al.			
	5,107,465	04/21/92	Fung et al.			
	4,206,833	04/27/93	Lee			
	4,953,128	08/28/90	Kawai et al.			
	5,140,688	08/18/92	White et al.			
	5,018,111	05/21/91	Madland			
	4,734,880	03/29/88	Collins			
	4,183,095	01/08/80	Ward			
	4,975,872	12/04/90	Zaiki			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

(3)	T.L. Jeremiah et. al., "SYNCHRONOUS PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. Disc. Bul,. Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982)
(4)	L. R. Metzeger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18 No. 5, pp. 562-567 (Oct. 1983)

EXAMINER Glenn Auvil	DATE CONSIDERED 5/29/2001

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	5,016,226	05/14/91	Hiwada et al.			
	5,109,498	04/28/92	Kamiya et al.			
	4,807,189	02/21/89	Pinkham et al.			
	4,092,665	05/30/78	Saran			
	4,799,199	01/17/89	Scales, III et al.			
	5,142,637	08/25/92	Harlin et al.			
	5,148,523	09/15/92	Harlin et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

(5)	A. Yuen et. al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989)
(6)	D.T. Wong et. al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5-μm Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988)
(7)	T. Williams et. al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988)
(8)	D. Jones, "Synchronous static ram", Electronics and Wireless World, vol.93, no.1622, pp. 1243-4 (Dec. 87)
(9)	F. Miller et. al., "HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMS", Midcon/87 Conference Record, pp. 430-432 Chicago, IL, USA; 15-17 Sept. 1987
(10)	K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986)
(11)	K. Nogami et. al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990)
(12)	F. Towler et. al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE international Solid State Circuits Conference, (Feb. 1989)

EXAMINER Glenn Auvil	DATE CONSIDERED 5/29/2001

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U.S. PATENT DOCUMENTS

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	5,016,226	05/14/91	Hiwada et al.			
	4,954,987	09/04/90	Auvinen et al.			
	4,675,850	06/23/87	Kumanoya et al.			
	4,788,667	11/29/88	Nakano et al.			
	4,945,516	07/31/90	Kashiyama			
	4,937,734	06/26/90	Bechtolsheim			
	4,845,664	07/04/89	Aichelmann, Jr. et al.			
	4,920,483	04/24/90	Pogue et al.			
	4,680,738	07/14/87	Tam			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

(13)	M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference
(14)	H. L. Kalter et al. "A 50-ns 16Mb DRAM with a 10-ns Data Rate and On-Chip ECC" IEEE Journal of Solid State Circuits, vol. 25 No. 5, pp. 1118-1128 (Oct 1990)
(15)	D. Wendell et. al. "A 3.5ns, 2Kx9 Self Timed SRAM", 1990 IEEE Symposium on VLSI Circuits (Feb 1990)
(16)	M. Bazes et. al., "A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. 18 No. 2, pp. 164-172 (Apr. 1983)
(17)	R. Schmidt, "A memory Control Chip fo Formatting Data into Blocks Suitable for Video Applications", IEEE Transactions on Circuits and Systems, vol. 36, No. 10 (Oct. 1989)
(18)	D. K. Morgan "The CVAX CMCTL – A CMOS Memory Controller Chip", Digital Technical Journal, No. 7 (Aug. 1988)
(19)	T.C. Poon et. al., "A CMOS DRAM-Controller Chip Implementation", IEEE Journal of Solid State Circuits, vol. 22 No. 3, pp. 491-494 (June 1987)
(20)	E.H. Frank "The SBUS: Sun's High Performance System Bus for RISC Workstations" Sun Microsystems Inc. 1990
(21)	K. Numata et. al. " New Nibbled-Page Architecture for High Density DRAM's", IEEE Journal of Solid State Circuits, vol. 24 No. 4, pp. 900-904 (Aug. 1989)

EXAMINER Glenn Auve	DATE CONSIDERED 5/29/2001

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	FILING DATE September 25, 2000	GROUP ART UNIT 2181

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	5,390,149	02/14/95	Vogley et al.			
	4,570,220	02/11/86	Tetrick et al.			
	5,083,296	01/21/92	Hara et al.			
	5,077,693	12/31/91	Hardee et al.			
	4,916,670	04/10/90	Suzuki et al.			
	4,247,817	1/27/81	Heller			
	5,301,278	04/05/94	Bowater et al.			
	4,970,418	11/13/90	Masterson			
	5,361,277	11/01/94	Grover			
	4,519,034	05/21/85	Smith et al.			
	4,315,308	02/09/82	Jackson			
	3,821,715	06/28/74	Hoff, Jr et al.			

FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER Glenn Anne	DATE CONSIDERED 5/29/2001

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,330,852	May 18, 1982	Redwiné et al.			
	4,703,418	Oct. 27, 1987	James			
	4,785,394	Nov. 15, 1988	Fischer			
	4,726,021	Feb. 16, 1988	Horiguchi et al.			
	4,870,562	Sept. 26, 1989	Kimoto et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
	S56-82961	July 7, 1981	Japan			YES	
	S57-14922	Jan. 26, 1982	Japan			YES	
	Sho 60-80193	May 8, 1983	Japan			YES	
	Sho 60-55459	Mar. 30, 1985	Japan			YES	
	S61-72350	April 14, 1986	Japan			YES	
	S63-142445	June 14, 1988	Japan			YES	
	B63-46864	Sept. 19, 1988	Japan			YES	
	S64-29951	Jan. 31, 1989	Japan			YES	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

(22)	(22)	Watanabe, T.; "Session XIX: High Density SRAMS"; IEEE International Solid State Circuits Conference pp. 266-267 (1987)
(23)		Ohno, C.; "Self-Timed RAM: STRAM"; Fujitsu Sci. TechJ., 24, 4, pp 293-300 (Dec. 1988)
(24)		"Fast Packet Bus for Microprocessor Systems with Caches", IBM Technical Disclosure Bulletin, pp.279-282 (Jan 1989)
(25)		Gustavson, D. "Scalable Coherent Interface"; Invited Paper, COMPCON Spring '89, San Francisco, CA; IEEE, pp. 536-538 (Feb 27-Mar 3, 1989)
(26)		James, D.; "Scalable I/O Architecture for Busses"; IEEE, pp. 539-544 (April 1989)

EXAMINER Glenn Auve	DATE CONSIDERED 5/29/2001

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
GM	4,205,373	May 27, 1980	Shah et al.			
GM	4,845,670	Jul. 4, 1989	Nishimoto et al.			
GM	4,509,142	Apr. 2, 1985	Childers			
GM	4,183,095	Jan. 8, 1980	Ward			
GM	4,685,088	Aug. 4, 1987	Ianucci			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
GM	0 246 767	April 28, 1987	EPO				
GM	0 334 552	Mar. 16, 1989	EPO				
GM	0 276 871	Jan. 29, 1988	EPO				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

(27) GM	European Search Report for EPO Patent Application No. 00 101 1832
(28) GM	European Search Report for EPO Patent Application No. 89 30 2613
(29) GM	Z. Amitai, "New System Architectures for DRAM Control and Error Correction", Monolithic Memories Inc., Electro/87 and Mini/Mico Northeast: Focusing on the OEM Conference Record, pp. 1132, 4/31-3, (April 1987)
(30) GM	N. Siddique, "100-MHz DRAM Controller Sparks Multiprocessor Designs", Electronic Design, pp. 138-141, (Sept 1986)
(31) GM	H. Kuriyama et al., "A 4-Mbit CMOS SRAM WITH 8-NS SERIAL ACCESS TIME" , IEEE Symposium On VLSI Circuits Digest Of Technical Papers, pp. 51-52, (June 1990)
(32) GM	J. Chun et al., "A 1.2ns GaAs 4K Read Only Memory", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 83-86, (Nov. 1988)
(33) GM	A. Fielder et al., "A 3 NS 1K X 4 STATIC SELF-TIMED GaAs RAM", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 67-70, (Nov. 1988)
(34) GM	JEDEC Standard No. 21C

EXAMINER Glenn Auve	DATE CONSIDERED 3/22/2001

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,630,193	Dec. 16, 1986	Kris			
	4,710,904	Dec. 1, 1987	Suzuki			
	4,739,502	Apr. 19, 1988	Nozaki			
	4,905,201	Feb. 27, 1990	Ohira et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

(35)	European Search Report for EPO Patent Application No. 00 10 0018
(36)	European Search Report for EPO Patent Application No. 00 10 822

EXAMINER Glenn Auvil	DATE CONSIDERED 5/22/2001

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#8

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA001C11	SERIAL NUMBER 09/669,295
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE September 25, 2000	GROUP ART UNIT 2181

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
[illegible]	4,755,937	July 5, 1988	Glier	—	—	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

✓ (1)	Grover et al., "Precision Time-Transfer in Transport Networks Using Digital Crossconnect Systems", IEEE Paper 47.2 Globecom, 1988, pp 1544-1548
✓ (2)	Knut Alnes, "Scalable Coherent Interface", SCI-Feb89-doc52, (To appear in Eurobus Conference Proceedings May 1989, pp. 1-8,
✓ (3)	Gustavson et al., "The Scalable Interface Project (Superbus)" (DRAFT), SCI-22 Aug 88-doc1 pp 1-16, August 22, 1988
✓ (4)	Moussouris, J. "The Advanced Systems Outlook-Life Beyond RISC: The next 30 years in high-performance computing", Computer Letter, July 31, 1989 (an edited excerpt from an address at the fourth annual conference on the Advanced Systems Outlook, in San Francisco, CA (June 5))
✓ (5)	Hansen et al., "A RISC MICROPROCESSOR WITH INTEGRAL MMU AND CACHE INTERFACE", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986 pp 145-148
✓ (6)	Moussouris et al., "A CMOS PROCESSOR WITH INTEGRATED SYSTEMS FUNCTIONS", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986 pp 126-130
✓ (7)	"LR2000 High Performance RISC Microprocessor Preliminary" LSI Logic Corp. 1988, pp. 1-15
✓ (8)	"LR2010 Floating Point Accelerator Preliminary" LSI Logic Corp. 1988, pp 1-20
✓ (9)	"High Speed CMOS Databook", Integrated Device Technology Inc. Santa Clara, CA, 1988 pp 9-1 to 9-9
✓ (10)	"IDT 79R2010 RISC Floating Point Accelerator (FPA) Advance Information", Integrated Device Technology Inc. Santa Clara, CA, 1987, pp. 9-10 to 9-14
✓ (11)	Riordan T. "MIPS R2000 Processor Interface 78-00005(C)", MIPS Computer Systems, Sunnyvale, CA, June 30, 1987, pp 1-83

EXAMINER Glenn Auve	DATE CONSIDERED 5/29/2001

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.